TEMIC Semiconductors

MATRA MHS

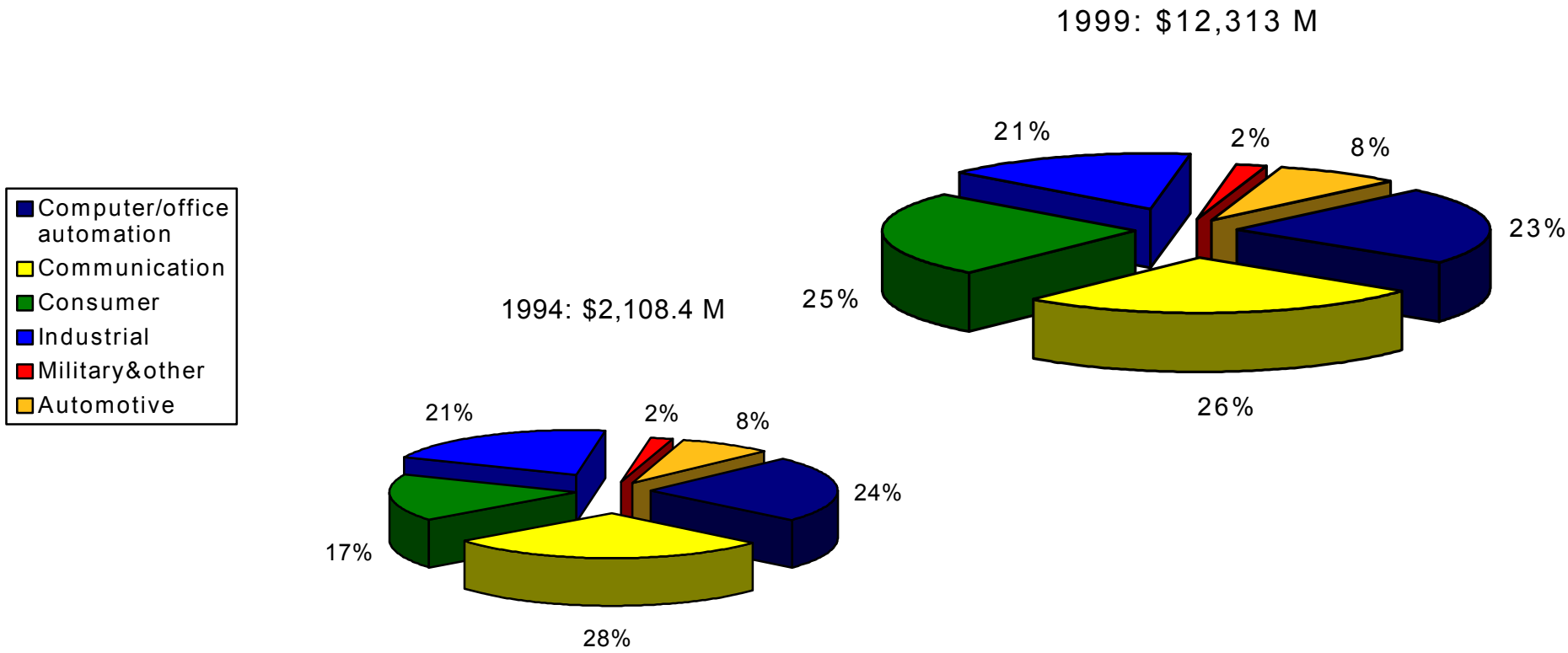
SPARClet™
32 bit RISC microcontroller family

Richard Pedreau-SPARC technical marketing
richard.pedreau@matramhs.fr

October 1995

A Company of AEG Daimler-Benz Industrie

Total WW High-End Embedded Processor Market

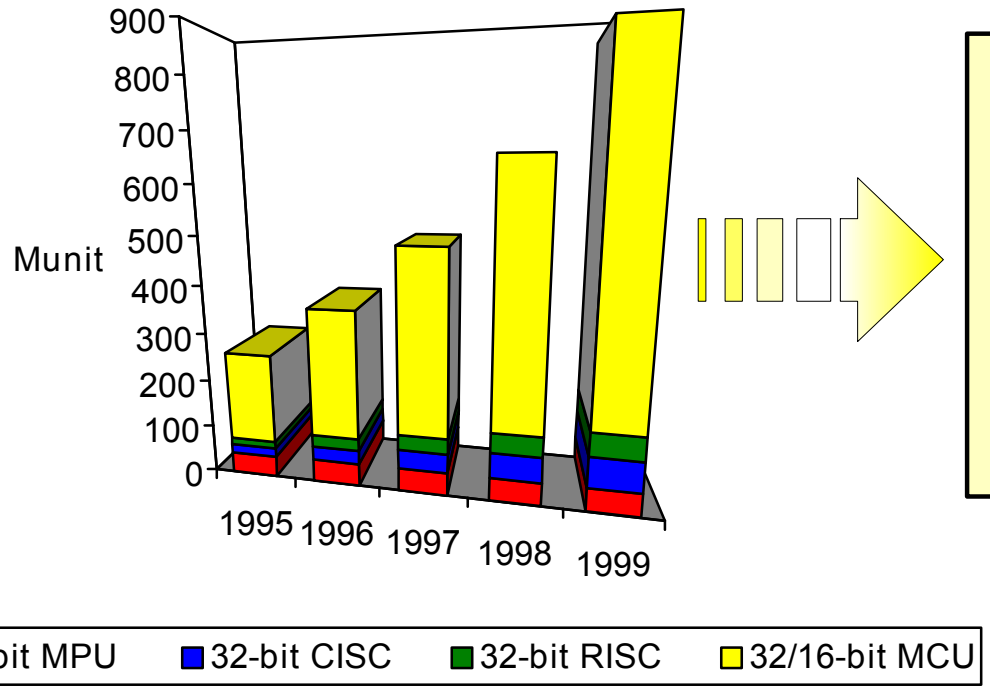


In-Stat June 1995

TEMIC market segments are:

Communication, Broadcast media, Computer/office automation, Automotive

Total WW Unit Shipments, High-End Embedded MPUs and MCUs



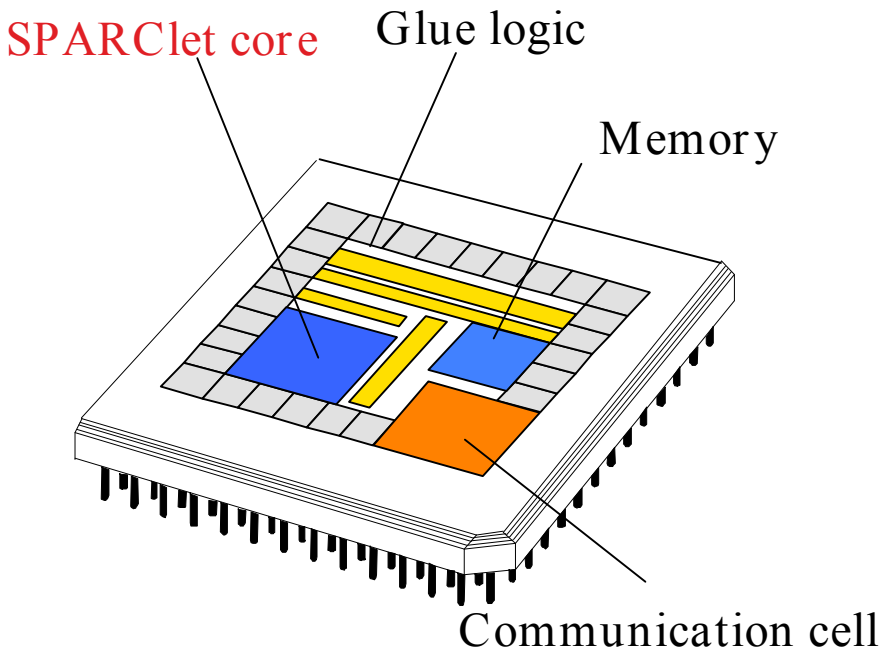
Digital Communication Systems
High Capicity Disk drives
Mobiles
Set top box
Car Electronic Systems
Fax/modem
.....

In-Stat June 1995

SPARClet™ Program Objectives

- to develop a processor core providing 32-Bit MCU + DSP + DMA capabilities in the range of 10$ to 30$ (as a cost core).
- to dedicate monochip solutions according to end-user requirements.
- to capitalize on popular platform (SUN/SPARC) by remaining compliant (SPARClet™/V8eR1).
- to reduce time to market for users and cost to market for vendors.

SPARClet™ Application Specific Monochip Solutions

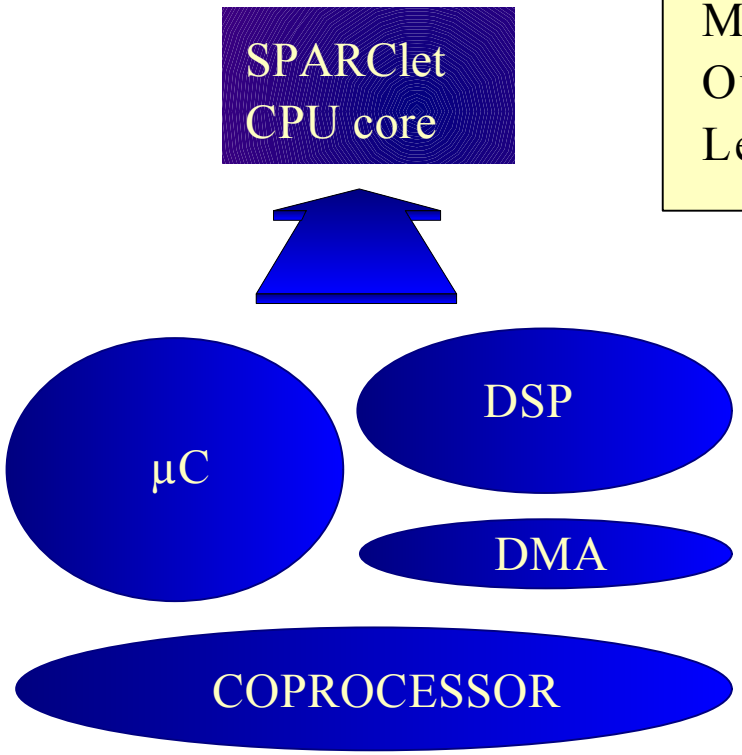


SPARClet™

- Reduction of the Customers Investment level
  - SPARC V8 Compliant
  - Software Third Party Program
  - Code generation Chain
- Improved SPARC Embedded Architecture
  - Digital Signal Processing Support
  - Parallel Processing (Scalar, Multiplication, load/store)
  - Fast Interrupt response time (Alternate Window registers)
  - High data flow throughput due to extended processor pipeline
- Reduced System Cost
  - DSP, control, and DMA functions in one CPU core.
  - Memory Latency time does not impact the performance

SPARClet™ Mixed digital signal and control processor unit

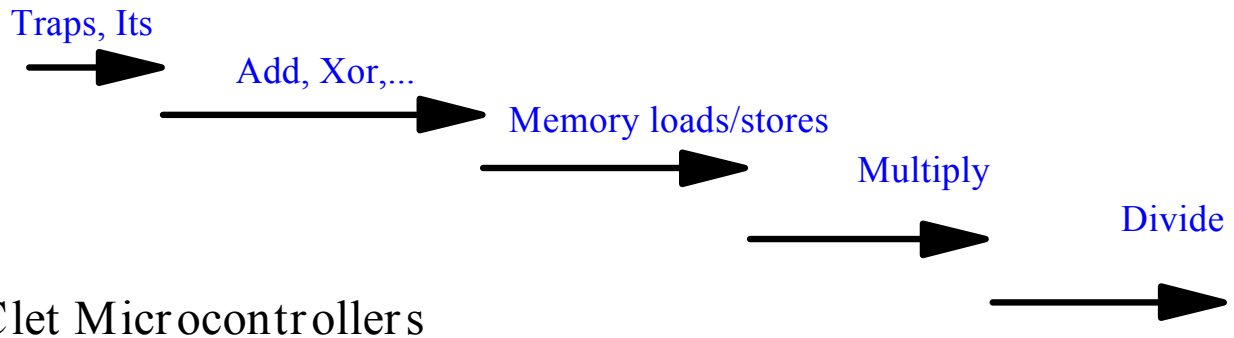
New Dedicated Instructions (14)
Parallel Processing
Co-processing
Dataflow Architecture
Modular & Parametrizable Architecture
Out-of-order instruction completion
Less than 6 mm2 for the minimal core on CMOS .6 µm



SPARClet™ - Architecture Principle

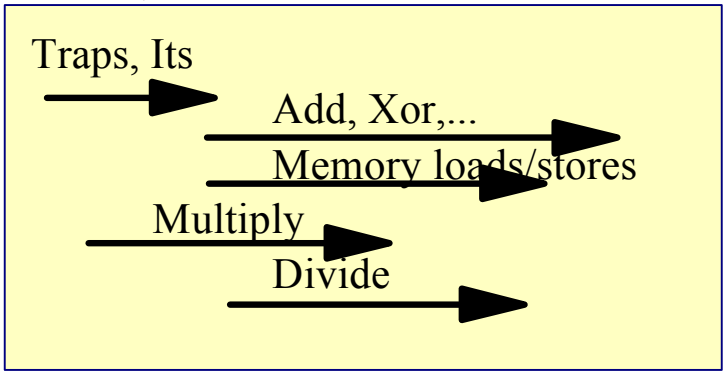
RISC Microprocessors & Microcontrollers

Time (iteration) = $\sum_{(time)}$ (interrupt service, scalar & Multicycle operations)

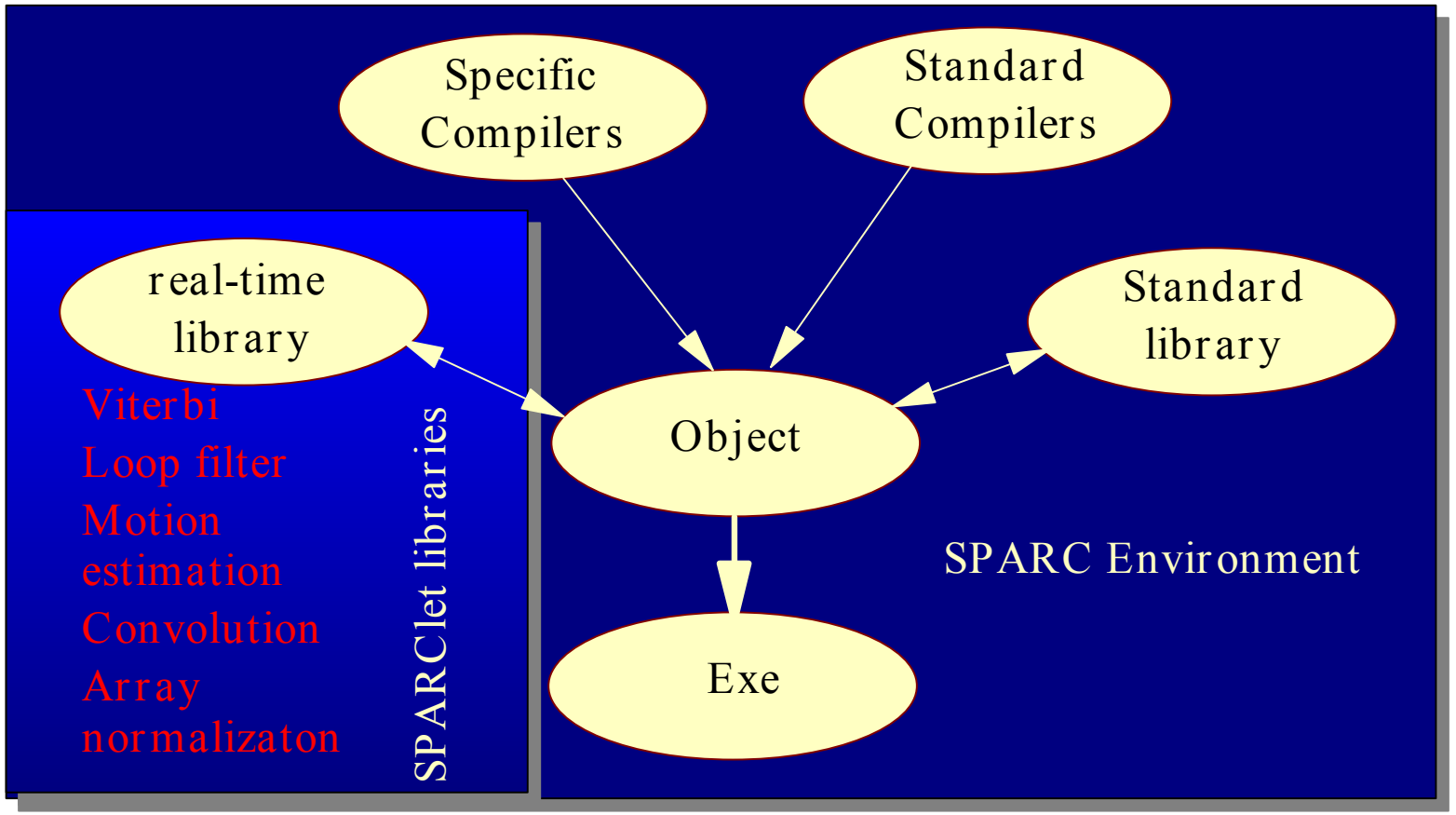


SPARClet Microcontrollers

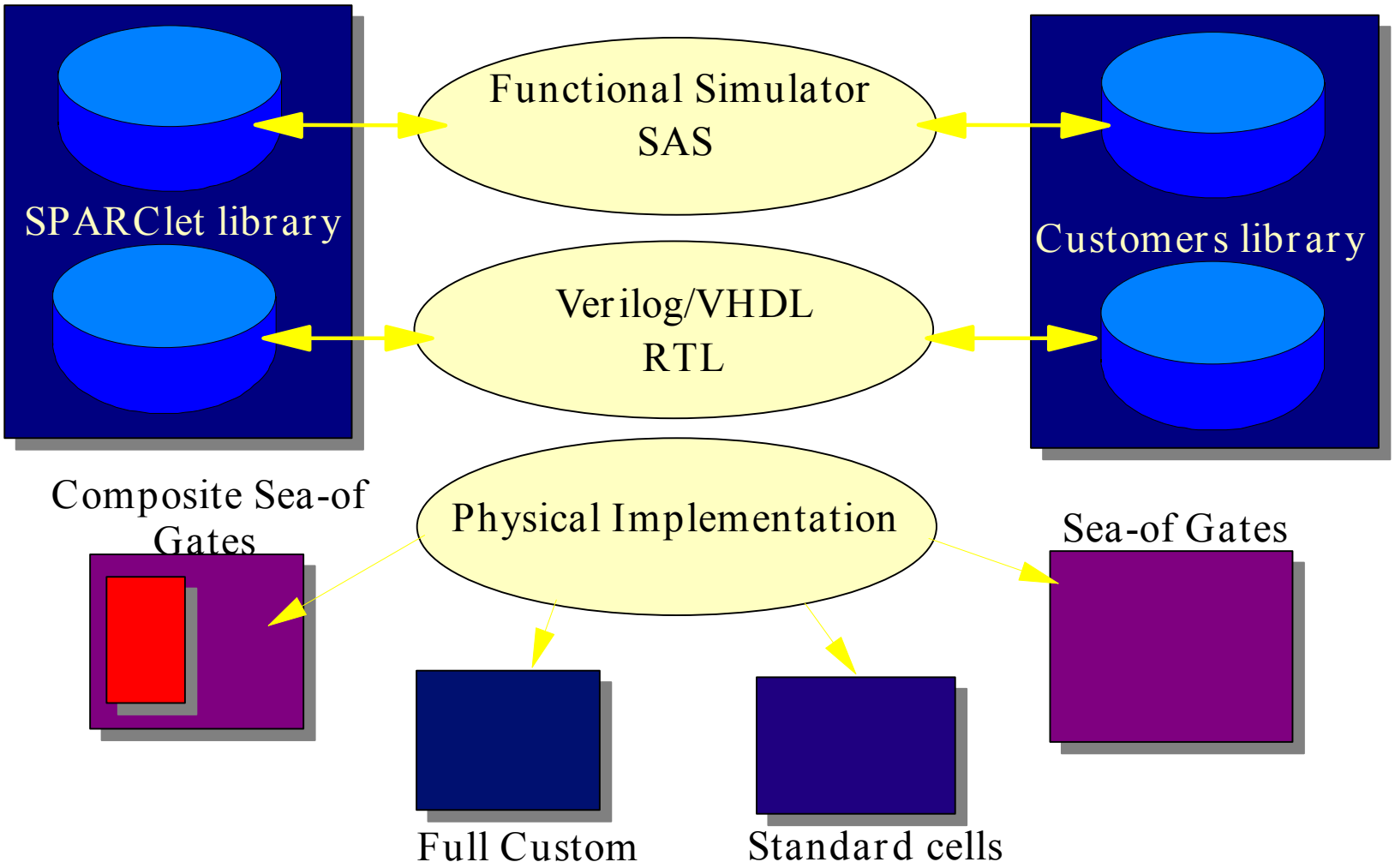
Time (iteration) = $MAX_{(time)}$ (interrupt service, scalar & Multicycle operations)



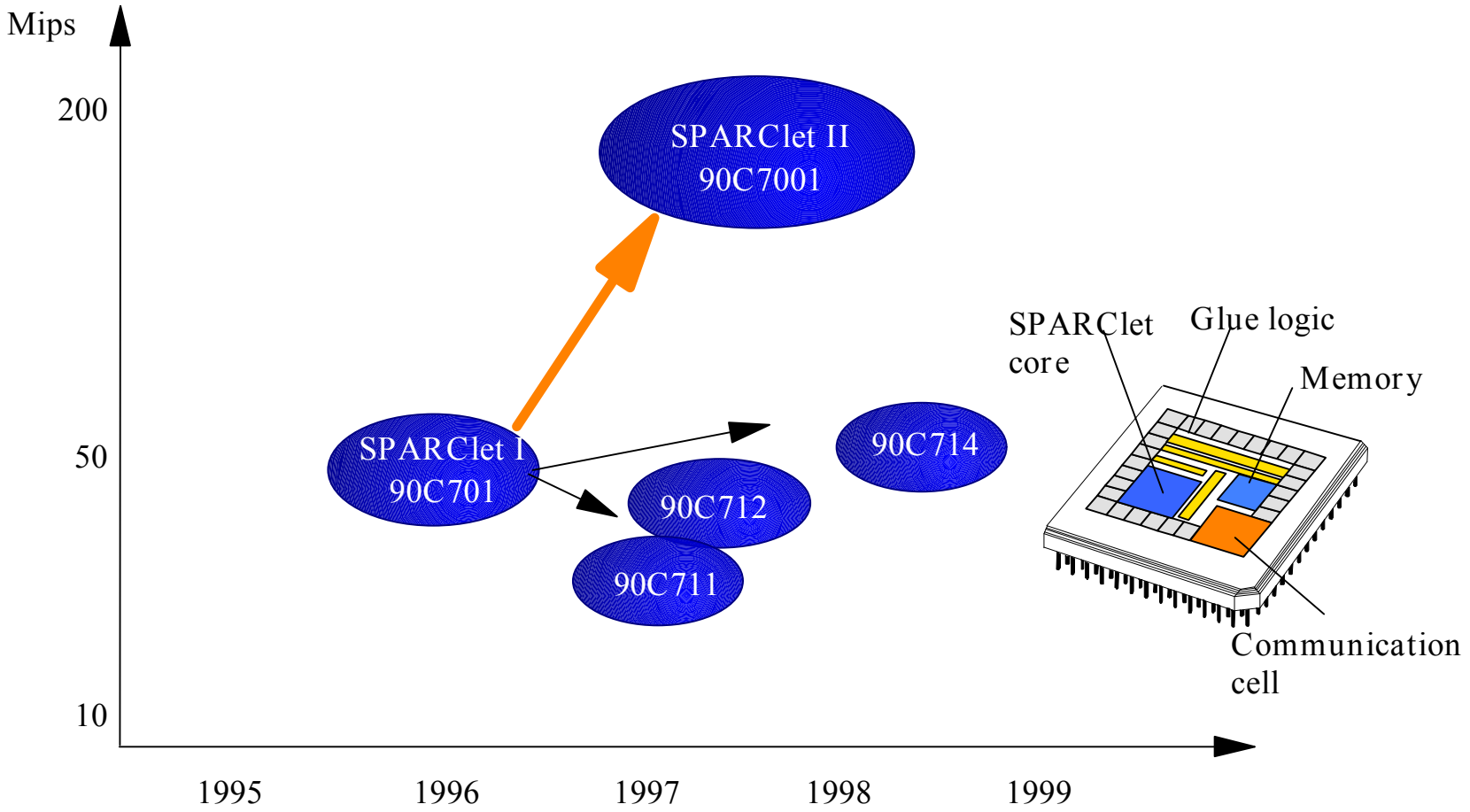
SPARClet™ Code generation issue



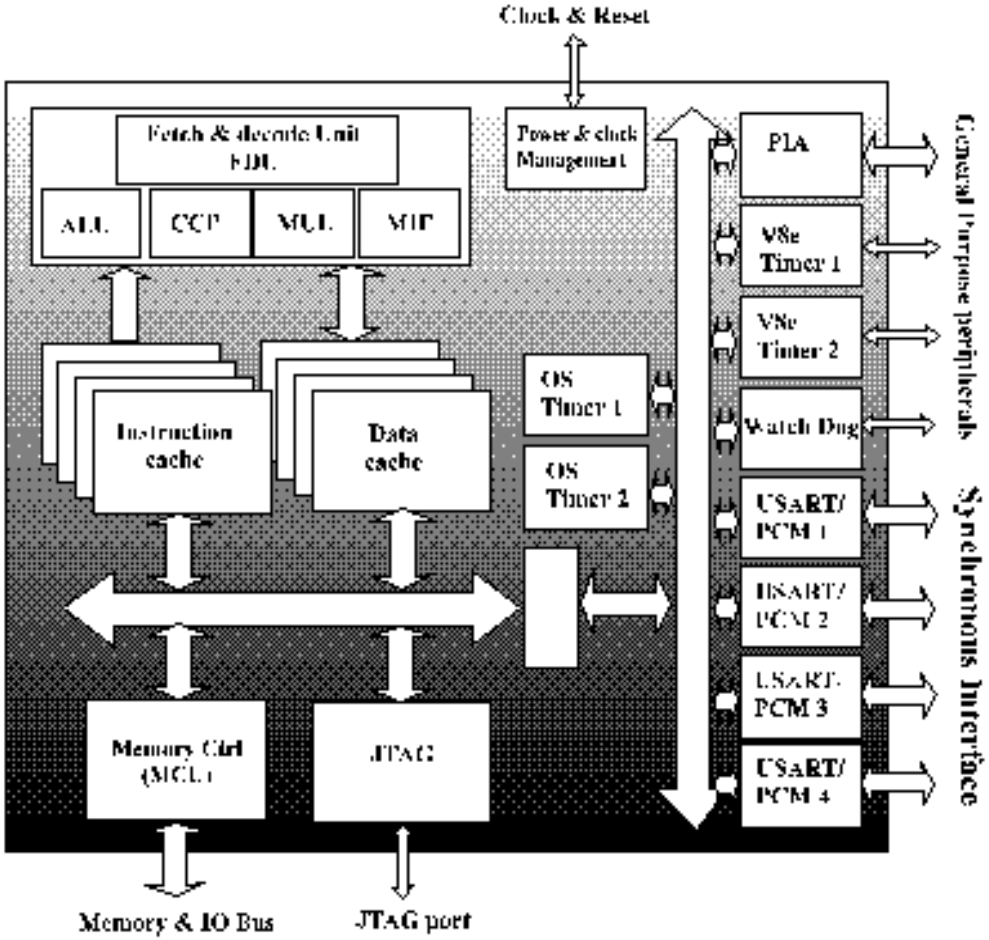
SPARClet™ Design Methodology



SPARClet™ Road Map



90C701: Advanced Communication Controller



-30 MHz @ 3.3 V (+-10%)
-50 Mhz @ 5 V (+-10%)
-Internal clock multiplier (x2)
-Fully Static SPARClet core
-Power Mgt techniques
-JTAG for debug & diag.
-0.6 µm CMOS, 3 MTL
-HDLC co-proc. up to 8 Mibts
-Up to four PCM links at 2Mbits
-Multiprocessor Support
-Allow glue less System
-208 PQFP - 240 PGA

Summary

- The 90C701 is an alternative solution to the Motorola PPC communication controller
  - SPARC V8 compliant
  - Software Third Party program
  - Performance/price ratio (50 to 100$)
  - Operational samples : 96Q1
- SPARClet is the optimal SPARC Embedded Solution
  - New design methodology reducing the cost and the time to market
  - Full parametrizable and modular CPU VHDL models
  - Small CPU core (6 mm2 on 0.6µm/3MTL) allowing low cost embedded systems
  - Fully Automatized VHDL to layout Design Environment